IN THE SPECIFICATION

Amend paragraphs 6, 10, 15, 18 - 21, 26, 44, 46, 54, 55, 66, 75, 98, 100, 101, 108, 119, 124, 173, 179, 181, 192, 193, 195, 202, 211, 212, 215, 222, 234, 238, 241, 250, 252, 254, 264, 292, and 305 as follows:

[0006] Fig. 1 illustrates a complementary-IGFET structure containing short-channel normally off n-channel surface-channel IGFET ("SCIGFET") 20 and short-channel normally off p-channel SCIGFET 22 created from a doped monocrystalline silicon ("monosilicon") semiconductor body as described in U.S. Patent 6,548,842 B1. The "SC" portion of the acronym "SCIGFET" means surface channel rather than short channel. Field region 24 of electrically insulating material extends into the semiconductor body along its upper surface to define a group of laterally separated active semiconductor regions. Item 26 in Fig. 1 illustrates lightly doped p-type monosilicon material that remains after SCIGFETs 20 and 22 are created.

[0010] Gate dielectric layer 60 lies on channel zone 52. Gate electrode 62 consisting of very heavily doped p-type polysilicon lies on gate dielectric layer 60 and extends laterally above part of each source/drain extension 50E. A pair of electrically insulating sidewalls spacers 64 are respectively situated along the opposite transverse sidewalls of p++ gate electrode 62. A metal silicide layer 66 is situated along the top of each main source/drain portion 50M. Further metal silicide layer 68 is situated along the top of gate electrode 62.

[0015] When the channel zone of an IGFET is of the same conductivity type as the source/drain zones, the channel zone is of opposite conductivity type to the body region and forms a channel-zone/body pn junction with the body region. An IGFET of this type can be a normally on device or a normally off device as described in Nishiuchi et al., "A Normally-off Type Buried-Channel MOSFET for VLSI Circuits", *IEDM Tech, Dig.*, Dec. ~~IEDM Dig. Tech. Paps.,~~ 1978, pp. 26 - 29. Referring to U.S. Patent 5,952,701, current conduction in such a normally off IGFET can occur along the upper surface of the channel zone or through a subsurface layer of the channel zone.

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[0018] CJIGFETs are often used in complementary-IGFET applications in which one of the two types of opposite-polarity IGFETs is a normally off CJIGFET while the other type is a surface-channel IGFET. In Hu et al., "Design and Fabrication of P-channel FET for 1-μm

CMOS Technology," *IEDM Tech, Dig.*, 11 - 15 Dec. ~~IEDM Tech. Dig.,~~ 1982, pages 710 - 713, the p-channel device is a normally off CJIGFET while the n-channel device is an SCIGFET. The opposite occurs in Parrillo et al., "A Fine-Line CMOS Technology That Uses P^+ Polysilicon/Silicide Gates for NMOS and PMOS Devices," *IEDM Tech, Dig.*, Dec. ~~IEDM Tech. Dig.,~~ 1984, pages 418 - 422.

[0019] SCIGFETs and normally off CJIGFETs have various advantages and disadvantages. For instance, an SCIGFET is typically easier to fabricate, especially with a threshold voltage that stays within desired limits at short channel length. On the other hand, a normally off CJIGFET typically has lower noise. See Hu et al., cited above, and Nishida et al., "SoC CMOS Technology for NBTI/HCI Immune I/O and Analog Circuits Implementing Surface and Buried Channel Structures", *IEDM Tech, Dig.*, 2 - 5 Dec. ~~IRPS Dig. Tech. Paps.,~~ 2001, pages. 39.4.1 - 39.4.4.

[0020] IGFETs, especially long-channel IGFETs, employed in analog circuitry ~~IGFETs employed in analog circuitry,~~ commonly operate across greater voltage ranges than short-channel IGFETs utilized in digital circuitry. As a result, the thickness of the gate dielectric layer of an IGFET designed for analog circuitry is often greater than the thickness of the gate dielectric layer of an IGFET designed for digital circuitry. In mixed-signal applications having both digital and analog circuitry, semiconductor fabrication processes commonly provide complementary IGFETs at two different gate dielectric thicknesses so that complementary IGFETs at a low gate dielectric thickness are available for the digital circuitry while complementary IGFETs at a high gate dielectric thickness are available for the analog circuitry.

[0021] Fig. 2 generally depicts a complementary-IGFET structure having a first pair of normally off complementary IGFETs 80 and 82 at one gate dielectric thickness and a second pair of normally off complementary IGFETs 84 and 86 at another (different) gate dielectric thickness as described in Nishida et al. cited above. Recessed electrically insulating field region 88 laterally separates the source/drain zones of each IGFET 80, 82, 84, or 86 from the source/drain zones of each other IGFET 80, 82, 84, or 86. Various wells (not shown) are provided in semiconductor body 90.

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[0026] The IGFET technology of the invention combines a normally off n-channel channel-junction IGFET (again, "CJIGFET") with an n-channel surface-channel IGFET (again, "SCIGFET"). The n-channel CJIGFET is normally of greater gate dielectric thickness than the n-channel SCIGFET so that the n-channel CJIGFET operates across a greater voltage range than the n-channel SCIGFET. The n-channel CJIGFET can conduct current by way of a field-induced surface channel or a metallurgical subsurface channel. In either case, the n-channel CJIGFET incurs much less, typically at least 90% less, 1/f noise than an otherwise substantially equivalent normally off n-channel surface-channel IGFET, i.e., an n-channel SCIGFET that operates across the same voltage range as the n-channel CJIGFET and thus across a greater voltage range than the n-channel SCIGFET used in the present technology.

[0044] Fig. 10 is a design chart for uniform net ~~average~~ channel-zone dopant concentration as a function of channel-zone junction depth for n-channel IGFETs at various conditions, including the condition at the crossover location between field-induced surface-channel conduction and metallurgical subsurface-channel conduction.

[0046] Figs. 12a - 12o, 12p.1 - 12x.1, and 12p.2 - 12x.2 are cross-sectional side structural views representing steps in manufacturing the complementary-IGFET structure of Figs. 3.1 and 3.2 in accordance with the invention. The steps of Figs. 12a - 12o apply to the structural portions illustrated in both of Figs. 3.1 and 3.2. ~~The steps of~~ Figs. 12p.1 - 12x.1 illustrate further steps leading to the structural portion of Fig. 3.1. ~~The steps of~~ Figs. 12p.2 - 12x.2 illustrate further steps leading to the structural portion of Fig. 3.2.

[0054] The present invention furnishes a complementary-IGFET ~~structure~~ semiconductor technology suitable for integrated circuits, such as mixed-signal devices having both analog and digital circuitry, which utilize complementary IGFETs that operate across two different voltage ranges. Figs. 3.1 and 3.2 (collectively "Fig. 3") illustrate two portions of an example of a complementary-IGFET structure which ~~that~~ employs the ~~that~~ complementary-IGFET technology of the invention. The complementary-IGFET structure of Fig. 3 contains a short-channel normally off n-channel surface-channel IGFET 100, a short-channel normally off p-channel surface-channel IGFET 102, a long-channel normally off n-channel channel-junction IGFET 104, and a long-channel normally off p-channel surface-channel IGFET 106.

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[0055] IGFETs 100, 102, 104, and 106 are situated along a major surface of a doped monosilicon semiconductor body. This surface is, for convenience, generally referred to here as the upper surface of the semiconductor body or simply the upper semiconductor surface. A recessed field region of electrically insulating material, typically primarily silicon oxide, extends into the upper semiconductor surface to define a group of laterally separated active semiconductor regions.

[0066] The long-channel version of each LV IGFET 100 or 102 receives the respective p-type or n-type halo dopant in the same manner as IGFET 100 or 102. The length of the channel zone in the long-channel version of IGFET 100 or 102 is sufficiently great that halo region 38 or 58 is replaced with a pair of laterally separated halo pocket portions. One of the halo pocket portions extends around one of the source/drain extensions (30E or 50E) to meet the associated main source/drain portion (30M or 50M). The other halo pocket extends around the other source/drain extension (30E or 50E) to meet the other main source/drain portion (30M or 50M). The long-channel version of IGFET 100 or 102 is otherwise configured the same as IGFET 100 or 102. Hence, the long-channel version of IGFET 100 or 102 appears as shown in Fig. 3.1 except that the length of channel zone 32 or 52 is sufficiently great that halo region 38 or 58 splits into ~~the~~ two ~~indicated~~ separate halo pockets.

[0075] The p-type device body material for IGFET 104 consists of a heavily doped well portion 114 and a moderately doped upper portion 116. P+ well portion 114 merges junctionlessly into p- material 26. P upper body-material portion 116 merges into well portion 114 and meets source/drain zones 110 ~~30~~ and channel zone 112 ~~32~~ to form the composite pn junction. Unlike IGFET 100, the p-type device body material for IGFET 104 does not include any halo-type region more heavily doped p-type than upper body-material portion 116 and extending around either n+ source/drain extension 110E.

[0098] The complementary-IGFET structure of Fig. 3 can be modified in various ways. Figs. 4 - 7 illustrate four ways of modifying either the LV structural portion of Fig. 3.1 or the HV structural portion of Fig. 3.2. The IGFET elements and other structural components in the modifications of ~~of if~~ Figs. 4 - 7 are identified with the same reference symbols used respectively for the corresponding IGFET elements and other structural components in Fig. 3 to the extent that the ~~these~~ elements and components in Figs. 4 - 7 are respectively the same or substantially the same as in Fig. 3.

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[0100] The p-type LV isolation dopant for IGFET 160 defines a heavily doped p-type intermediate body-material portion 164 that lies between, and merges into, p+ well portion 34 and p upper body-material portion 36. The n-type LV isolation dopant for IGFET 162 similarly defines a heavily doped n-type intermediate body-material portion 166 that lies between, and merges into, n+ well 54 and n upper body-material portion 56. ~~156.~~ While intermediate body-material portions 164 and 166 are described here as heavily doped, they could alternatively be described as moderately doped. P+ well portion 34 and p+ intermediate portion 164 form a composite p-type LV well 34/164 for IGFET 160. N+ well portion 54 and n+ intermediate portion 166 form a composite n-type LV well 54/166 for IGFET 162.

[0101] The p-type LV isolation dopant causes the net dopant concentration for the p-type device body material of IGFET 160 to reach, in intermediate body-material portion 164, an additional local subsurface maximum at a location between the locations ~~location~~ for the primary (APT) and further (well) local subsurface maxima in the net dopant concentration for that p-type body material. The n-type LV isolation dopant similarly causes the net dopant concentration for the n-type device body material of IGFET 162 to reach, in intermediate body-material portion 166, an additional local subsurface maximum at a location between the locations ~~location~~ for the primary (APT) and further (well) local subsurface maxima in the net dopant concentration for that n-type body material. The additional local subsurface maxima in the net dopant concentration for the body materials of IGFETs 160 and 162 each normally occur 0.3 - 0.5 μm below the upper semiconductor surface, typically 0.4 μm below the upper semiconductor surface, when the channel lengths of IGFETs 160 and 162 are defined according to lithographic design rules whose minimum printable feature size is 0.25 μm or less, e.g., 0.18 μm.

[0108] In an FIC embodiment, CJIGFET 184 conducts current through an electrically conductive channel induced in a layer of channel zone 186 extending along the upper semiconductor surface from source-acting source/drain zone 130 to drain-acting source/drain zone 130 so that IGFET 184 is ~~as to be~~ turned on when the gate-to-source voltage is less than the negative threshold voltage. The induced surface channel consists of holes attracted to the upper surface of channel zone 186 by the transversal electric field that arises from having the gate-to-source voltage be less than or equal to the negative threshold voltage. The channel-

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side portion of the depletion region extending along the pn junction between channel zone ~~zones~~ 186 and upper body-material portion 136 occupies the remainder of channel zone 186. Raising the gate-to-source voltage to a value above the negative threshold voltage of IGFET 184 causes the surface channel to disappear, thereby turning IGFET 184 off. The channel-side portion of the junction depletion region then occupies all of channel zone 186.

[0119] The threshold voltage of n-channel CJIGFET 104 can be at a value somewhat different from 0.6 V in the simplified design model of Fig. 8. Based on Fig. 8, ~~the~~ threshold voltage V_{T0} of IGFET 104 for normally off operation with a metallurgical channel is 0.2 - 0.8 V, typically 0.6 V. As in the actual implementation of IGFET 104, thickness y_J of channel zone 112 is then 0.05 - 0.15 μm, typically 0.1 μm, provided that the combination of the V_{T0}, y_J, t_{GD}, N_C, N_B, and N_{POLY} values places IGFET 104 in the normally off MC regime.

[0124] The parameter values for CJIGFET 104 can be chosen so as to operate clearly within the FIC regime rather than on the boundary between the FIC and MC parameter regimes. Based on Fig. 8, ~~the~~ threshold voltage V_{T0} of IGFET 104 for (normally off) FIC operation is 1.0 - 1.2 V. As with ~~the~~ threshold voltage V_{T0} for the MC embodiment, this V_{T0} range ~~these V_T values~~ for the modeled FIC embodiment of IGFET 104 differs ~~differ~~ slightly from the V_T range ~~values~~ prescribed above for IGFET 104 due to the V_{T0} reduction caused by the reverse short-channel effect. Corresponding thickness y_J of channel zone 112 for the FIC embodiment is 0.02 - 0.10 μm, typically 0.05 μm, provided that the combination of V_{T0}, y_J, t_{GD}, N_C, N_B, and N_{POLY} values places IGFET 104 in the FIC regime or along the MC/FIC boundary.

[0173] A moderately doped precursor upper body-material portion 116P for IGFET 104 is defined by ion implanting a species of the p-type HV APT dopant ~~dopant,~~ at a moderate dosage through the uncovered section of screen oxide 202 and into epitaxial layer 26P. The dosage of the p-type HV APT dopant is 2×10^{12} - 6×10^{12} ions/cm^2, typically 4×10^{12} ions/cm^2. The p-type HV APT dopant may consist of boron in elemental form or in the form of boron difluoride. For the typical case in which elemental boron constitutes the p-type HV APT dopant, the implantation energy is 40 - 60 keV, typically 50 keV. The lightly doped remainder of epitaxial layer 26P is p- material 26 after completion of the p-type HV well and APT doping operations.

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[0179] A thermal anneal is optionally now performed on the resultant semiconductor structure to repair lattice damage and place the implanted n-type and p-type dopants in energetically more stable sites so as to minimize further diffusion of these dopants during subsequent thermal operations, especially the final anneal described below. This optional intermediate anneal is preferably a rapid thermal anneal ("RTA") at 900 - 1100°C, typically 1000°C, for 5 - 20 sec., typically 10 sec. The RTA is normally done in a non-reactive environment, typically nitrogen, but can be done in a reactive, e.g., oxidizing, environment. By using the RTA, the implanted dopants are activated without significant dopant movement (redistribution). Although the above-mentioned implantation steps define precursor channel-zone portion 112P, precursor upper body-material portions 38P, 56P, 116P, and 136P, ~~and~~ well portions 34, 54, 114, and 134 and, in variations of the complementary-IGFET structure of Fig. 3, deep well portion 182 for HV IGFET 180 or 190, the precursor to channel zone 186 for HV IGFET 184 or 190, and intermediate body-material portions 164 and 166 respectively for LV IGFETs 160 and 162, the intermediate anneal completes the formation of these regions.

[0181] Subsequent to the intermediate anneal, screen-oxide layer 202 is removed to expose the upper semiconductor surface as shown in Fig. 12h. The upper semiconductor surface is also cleaned, typically by a wet chemical process utilizing various combinations of strong acid, hydrogen peroxide, deionized water, and possibly ammonium hydroxide. The acid is typically sulfuric or/and hydrochloric acid. In one embodiment, the cleaning step is performed with 98 % sulfuric acid and 2% hydrogen peroxide at 120°C for 10 min. The cleaning step removes surface contaminants along with a few atomic layers of the exposed silicon to provide a clean upper semiconductor surface in order to help reduce noise.

[0192] A typical thermal schedule for growing thin dielectric layer 218 to a target thickness of approximately 4 nm and increasing the thickness of thick dielectric remainder 214R consists of a ramp-up from 700°C to 750°C at 15°C/min. in nitrogen with 1% oxygen, a stabilization at 750°C for 10 min. in nitrogen with 1% oxygen, a thermal oxidation at 750°C for 20 - 30 min., typically 25 min., in hydrogen and oxygen diluted 90% in argon, a stabilization at 750°C for 10 min. in nitrogen, a ramp-up from 750°C to 900°C at 10°C/min. in argon, an anneal at 900°C for 10 - 15 min., typically 10 min., in argon, and a ramp-down from 900°C to 600°C in argon. Based on suitable experimentation, other target thicknesses

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for dielectric layer 218 are achieved by adjusting certain portions of the thermal schedule, e.g., the length of the thermal oxidation at 750°C. For instance, reducing the duration of the 750°C thermal oxidation by 10 - 15 % leads to a target thin dielectric thickness of approximately 3.5 nm, the typical thickness value of gate dielectric layers 40 and 60 for operating IGFETs 100 and 102 at 1.8 ~~5.0~~ V.

[0193] The anneal at 900°C for growing thin dielectric layer 218 and increasing the thickness of thick dielectric remainder 218R can alternatively be done in nitrogen or nitrous oxide. The ramp-up to, and the ramp-down from, the 900°C anneal are then typically done in nitrogen. The 900°C anneal in argon, nitrogen, or nitrous oxide determines whether dielectric layer 218 consists of silicon oxide or silicon oxynitride. When the 900°C anneal is done in argon or nitrogen, ~~the~~ layer 218 consists substantially of silicon oxide. Layer 218 consists of silicon oxynitride when the 900°C anneal is done in nitrous oxide. This occurs because nitrous oxide is much more reactive than argon and nitrogen and results in nitrogen being introduced into layer 218. The increased-thickness portions of dielectric remainder 214R are constituted the same as dielectric layer 218.

[0195] Referring to Fig. 12m, a layer 220 of largely undoped (intrinsic) polysilicon is deposited on thick dielectric remainder 214R and thin dielectric layer 218 to a thickness of 200 - 300 nm, typically 250 nm. A photoresist mask 222 is formed on polysilicon layer 220. See Fig. 12n. ~~12m.~~ An opening extends through mask 222 above the active region for each of HV IGFETs 104 and 106.

[0202] Returning to Fig. 12, a patterning operation is performed on p++ material 220D and remainder 220R of polysilicon layer 220 to define the lateral shapes for gate electrodes 42, 62, 122, and 142. In particular, a photoresist mask 224 is formed on polysilicon material 220D and polysilicon remainder 220R. See Fig. 12o. ~~12a.~~ Mask 224 covers the portions of material 220D and remainder 220R at the intended locations for gate electrodes 42, 62, 122, and 142. The uncovered material of material 220D and remainder 220R is removed. The remaining portions 42P and 62P of polysilicon remainder 220R are respective largely undoped precursors to gate electrodes 42 and 62 of LV IGFETs 100 and 102. Remaining portions 122P and 142P of material 220D are respective p++ precursors to gate electrodes 122 and 142 of HV IGFETs 104 and 106.

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[0211] The uncovered material of second polysilicon layer 232 is removed as indicated in Fig. 13e. Item 232R is the remainder of polysilicon layer 232. Barrier dielectric layer 230 acts as a barrier (etch stop) to prevent first polysilicon remainder 226R from being attacked (and substantially removed) by the etchant utilized to remove the uncovered material of polysilicon layer 232. In the course of etching polysilicon layer 232, a parasitic polysilicon spacer may remain along the side edge of barrier layer 230. If formed, this polysilicon spacer ~~layer~~ can readily be removed, e.g., by extending the etch time for etching polysilicon layer 232 beyond the point at which the upper surface of barrier layer 230 is fully exposed. Accordingly, the polysilicon spacer is not shown in the drawings.

[0212] Barrier dielectric layer 230 is subsequently removed with etchant that does not significantly attack first polysilicon remainder 226R. Because barrier layer 230 covered ~~covers~~ the side edges of first polysilicon remainder 226R, polysilicon remainders 232R and 226R are laterally separated from each other by space above field insulation 24.

[0215] The patterning operation is initiated by forming ~~forming a~~ photoresist mask 224 on polysilicon remainders 226R and 232R. Mask 224 covers the portions of second polysilicon remainder 232R at the intended locations for gate electrodes 42 and 62 and the portions of first polysilicon remainder 226R at the intended locations for gate electrodes 122 and 142. The uncovered material of polysilicon portions 226R and 232R is removed. The remaining largely undoped portions of second polysilicon remainder 232R are then precursor gate electrodes 42P and 62P of LV IGFETs 100 and 102. The remaining p++ portions of first polysilicon remainder 226R are precursor gate electrodes 122P and 142P of HV IGFETs 104 and 106. The structure processed according to the alternative of Fig. 13 now appears substantially as shown in Fig. 12o.

[0222] For the long-channel version of p-channel LV IGFET 102, ions of the species of the n-type halo dopant are implanted through uncovered portions of surface dielectric layer 238 and into a pair of laterally separated surface-adjoining segments of n upper body-material portion 56P to define a pair of laterally separated heavily doped n-type precursor halo pocket portions. In either case, the material consisting of photoresist mask 240, field insulation 24, gate electrode 62P, and the portion of seal oxide 236 situated along electrode 62P forms a shield which largely blocks the n-type halo dopant from simultaneously passing through the upper semiconductor surface section directly underlying the shield.

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[0234] Similar to what occurs in the n-type angled halo implantation for p-channel IGFET 102, the tilted implantation of the p-type halo dopant at two largely opposite azimuthal angles causes ions of the p-type halo-dopant species to penetrate below precursor gate electrode 42P of n-channel IGFET 100 into a pair of portions of the intended location of channel zone 32 ~~zone 38~~ along both transverse sides of gate electrode 42P. The ions passing along one of the transverse sides of gate electrode 42P accumulate in one precursor halo pocket portion that extends below electrode 42P along that transverse gate-electrode electrode side. The ions passing along the other transverse side of electrode 42P accumulate in another precursor halo pocket portion that extends below electrode 42P along the other transverse gate-electrode side. The channel length of IGFET 100 is sufficiently small that these two precursor halo pocket portions merge together under gate electrode 42P to form p+ precursor halo region 38P. The long-channel version of IGFET 100 is of sufficiently great channel length that these two precursor halo pocket portions are spaced apart from each other. Also similar to what occurs in the n-type angled halo implantation for IGFET 102, substantially the same results arise when the number M_A of azimuthal angles for the p-type angled halo implantation is an even number greater than 2.

]0238] The total dose of the p-type HV source/drain extension dopant is 1×10^{13} - 4×10^{13} ions/cm^2, typically 2×10^{13} ions/cm^2, regardless of the number M_A of azimuthal angles. One fourth of the p-type HV source/drain extension dosage is preferably furnished at each azimuthal angle in the preferred case where M_A is 4. The p-type HV source/drain extension dopant may consist of boron in the form of boron difluoride or in elemental form. For the typical case in which boron difluoride constitutes the p-type HV source/drain extension dopant, the implantation energy is 20 - 50 keV, typically 30 keV. Photoresist 244 is removed subsequent to the p-type HV source/drain extension implantation.

[0241] The total dose of the n-type HV source/drain extension dopant is 1×10^{13} - 3×10^{13} ions/cm^2, typically 2×10^{13} ions/cm^2, regardless of the number M_A of azimuthal angles. One fourth of the n-type HV source/drain extension dopant is preferably furnished at each azimuthal angle in the preferred case where M_A is 4. The n-type HV source/drain extension dopant may consist of phosphorus or arsenic. For the typical case in which phosphorus constitutes the n-type HV source/drain extension dopant, the implantation energy is 40 - 80

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keV, typically 60 keV. Photoresist 246 is removed subsequent to the n-type HV source/drain extension implantation.

[0250] Due to the presence of sidewall spacers 44, n++ main source/drain portions 30M for IGFET 100 respectively partially overlap n+ source/drain extensions 30EP. The presence of sidewall spacers 124 similarly results in n++ main source/drain portions 110M for IGFET 104 respectively partially overlapping n+ source/drain extensions 110EP. Main source/drain portions 30M and 110M are doped much heavier n-type than, and respectively extend deeper into ~~into,~~ upper body-material portions 36P and 116P than, ~~than~~ precursor drain extensions 30EP and 110EP. Hence, the heavily doped n-type remainders of precursor extensions 30EP and 110EP respectively constitute n+ source/drain extensions 30E and 110E. The moderately doped p-type remainders of upper body-material portions 36P and 116P now respectively constitute p upper body-material portions 36 and 116. The p+ remainder of precursor halo region 38P now constitutes p+ halo region 38. The moderately doped n-type remainder of precursor channel zone 112P is now n channel zone 112.

[0252] Precursor gate electrode 122P of CJIGFET 104 received the very heavy dosage of the n-type main source/drain implantation. Some p-type and n-type dopant was also introduced into gate electrode 122P during the p-type and n-type doping operations conducted prior to the n-type main source/drain implantation but subsequent to the p-type HV gate implantation. The amount of n-type dopant introduced into electrode 122P during the doping operations performed between the p-type HV gate implantation and the n-type main source/drain implantation is insignificant compared to the amount of n-type dopant that electrode 122P received during the n-type main source/drain implantation. By satisfying Inequality 5, the amount of p-type dopant that electrode 122P received during the p-type HV gate implantation is considerably greater than the amount of all other n-type dopant, including the very heavy dosage of the n-type main source/drain implantation, received by electrode 122P. Accordingly, precursor electrode 122P remains very heavily doped p-type and is now p++ gate electrode 122 of IGFET 104. Importantly, gate electrode 122 is of opposite conductivity type to n-type source/drain regions 110 and n channel zone 112 as is typically desirable for a channel-junction IGFET.

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[0254] The material consisting of photoresist mask 254, field insulation 24, precursor gate electrode 62P, and sidewall spacers 64 forms, for IGFET 102, a shield that largely

blocks the p-type main source/drain dopant from passing through the upper semiconductor surface section directly below the shield. The material consisting of mask 254, field insulation 24, precursor gate electrode 142P, and sidewall spacers 144 ~~spacers 44~~ similarly forms, for IGFET 106, a further shield that largely blocks the p-type main source/drain dopant from passing through the upper semiconductor surface section directly below the further shield.

[0264] The thin layers of dielectric material, including dielectric layers 248 and 250, ~~236 and 238,~~ are removed along the upper semiconductor surface and along the top surfaces of gate electrodes 42, 62, 122, and 142. Field insulation 24 and spacers 44, 64, 124, and 144 remain substantially in place.

[0292] Thick dielectric layer 214R and thin dielectric layer 218, whether created according to the steps of Figs. 12k - 12m or the steps of Figs. 13a - 13d, together form a multiple-thickness gate-dielectric-containing dielectric layer (214R/218) whose thickness is (a) comparatively low at the lateral locations for gate dielectric layers 40 and 60 of LV IGFETs 100 and 102 and their respective LV variations 160 and 162 and (b) comparatively high at the lateral locations for gate dielectric layers 120 and 140 of HV IGFETs 104 and 106 and ~~and the~~ HV variations 180, 184, and 190 of IGFET 106. Instead of creating this multiple-thickness dielectric layer according to the dual dielectric-growth procedure of Figs. 12k - 12m or the dual dielectric-growth procedure of Figs. 13a - 13d, the multiple-thickness dielectric layer can be created by substantially a single dielectric-growth procedure in which the thermal growth of the multiple-thickness dielectric layer is suitably retarded at the locations for gate dielectric layers 40 and 60 or/and suitably enhanced at the locations for dielectric layers 120 and 140.

[0305] The lower heavily doped p-type source/drain portions for p-channel IGFETs 102 and 106 are similarly created using photoresist mask 254 (see Fig. 12x) by ion implanting a species of a p-type semiconductor dopant, referred to here as the p-type lower source/drain dopant, through the uncovered portions of surface dielectric layer 248 into ~~in~~ n upper body-material portions 56 and 136 (or 56P and 136P). The p-type lower source/drain dopant is ion implanted to a greater average depth than, but at a lower dosage than, the p-type main source/drain dopant. The portions of the n-type and p-type dopants underlying main

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source/drain portions 30M, 50M, 110M, and 130M constitute the lower source/drain portions to achieve the graded-junction characteristic.

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